UDC 621.397.63:
621.377

BBC

RESEARCH DEPARTMENT

1968
THE QUEEN'S AWARD
TO INDUSTRY

REPORT

Field-store standards conversion: the development of variable-delay timing correctors

No. 1972/5

Research Department, Engineering Division
THE BRITISH BROADCASTING CORPORATION

RESEARCH DEPARTMENT

FIELD-STORE STANDARDS CONVERSION: THE DEVELOPMENT OF VARIABLE-DELAY TIMING CORRECTORS

Research Department Report No. **1972/5**
UDC 621.397.63:
621.377

It uses SI units in accordance with B.S. document PD 5686.

D.W. Osborne, C. Eng., M.I.E.E.
A. Roberts, B. Eng.

P. Lanigan

Head of Research Department

EL-59

Research Department Report No. 1972/5

FIELD-STORE STANDARDS CONVERSION: THE DEVELOPMENT OF VARIABLE-DELAY TIMING CORRECTORS

Section	Title	Page
	Summary	1
1.	Introduction	1
2.	The reasons for replacing the line-store timing corrector	1
3.	The new timing corrector – broad design philosophy	2
4.	The problems when synchronising PAL-coded colour signals	3
5.	Description of each stage	4
	5.1. Timing Corrector 1 (TC1)	4
	5.2. Timing Corrector 2 (TC2)	5
	5.3. Timing Corrector 3 (TC3)	6
	5.4. Timing Corrector 2A (TC2A)	6
6.	Conclusions	7
7.	References	8

March 1972

Research Department Report No. 1972/5
UDC 621.397.63:
621.377

FIELD-STORE STANDARDS CONVERSION: THE DEVELOPMENT OF VARIABLE-DELAY TIMING CORRECTORS

Summary

The need for the development of new timing correctors for the BBC C06/508 field-store converter/synchroniser is discussed and outline descriptions of each stage of the timing corrector are given. The corrector consists essentially of a variable delay which is automatically adjusted at the beginning of each television line to reduce perturbations of up to ±16 μs in the timing of the input signal to a target accuracy of ±1 ns for the output signal.

1. Introduction

The basic conversion process in the C06/508 field-store television standards converter[1,2] is carried out by means of a system of switched ultrasonic, fused-quartz delay lines. The signal resulting from this process has the correct mean line frequency of the output standard but, because of the small difference between input and output line frequencies and because of delay and timing errors in the system of delay lines, the output television lines are irregularly timed. A timing corrector is therefore necessary to produce precisely-timed television lines suitable for broadcasting. The timing correctors must accept an input signal timing error range of up to about ±16 μs and reduce this to about ±10 ns for monochrome operation or about ±1 ns for colour operation.

An earlier field-store converter[3] (the C06/506 equipment) uses a line-store[4] type of timing corrector* in which picture-element samples of the input video signal are temporarily stored in capacitors until 'read' out at the required time for the output signal. The second converter (the C06/508 equipment)[5] also used a line-store timing corrector for the first few months of operation in the Television Service, but this was a temporary expedient to meet a service target date. Because of the planned later development of the converter to function alternatively as a synchroniser,[6] the line-store timing corrector was ultimately replaced with a specially-developed timing corrector which is the subject of this report.

2. The reasons for replacing the line-store timing corrector

It is not possible to pass a composite colour video signal through the existing form of line-store timing corrector without introducing severe impairment. The process of 'writing' and 'reading' signal samples into and out of the stores is insufficiently precise, with the result that serious delay and amplitude perturbations of the chrominance signal occur. In addition the clock-pulse sampling frequency is insufficiently high to describe the higher sidebands of the chrominance signal and, because of the relatively high energy of the high-frequency chrominance components, beats with the clock pulses are visible on the output picture. Difficulties also arise with the 'write' and 'read' clock-pulse frequencies; unless these are rigidly related the output subcarrier frequency will be incorrect, thus introducing problems in the subsequent decoding of the signal.

These difficulties were avoided in the field-store converter, in its original form, by first decoding the colour signal from the Main Store** into luminance and two colour-difference signals, and then using, in effect, three separate line-store timing correctors. This solution was temporarily acceptable since transcoding (decoding and then re-encoding) to the required output standard was an essential part of the conversion process. When operating as a synchroniser, however, transcoding is not required. Decoding to luminance and colour-difference signals could have been adopted in order to be able to continue using the line-store timing corrector, but it was felt to be unacceptable on account of the inevitable loss of vertical chrominance definition and the general signal degradation which would be introduced.

Further, minor, reasons for replacing the line-store timing corrector were that routine adjustments were necessary to keep the characteristic vertical striations to an acceptably low level and also reliability was felt to be somewhat inadequate.***

* In fact a modified line-store standards converter.

** The Main Store is the system of switched delay lines in which the basic conversion process of changing the number of lines per field and the number of fields per second is carried out.

*** Some 27 line-store converters are still used in the BBC to provide the duplicate 405-line v.h.f. transmissions of the BBC1 programme but, largely for the reasons stated, it is planned to replace these with converters, now being developed, which employ digital techniques.[7]

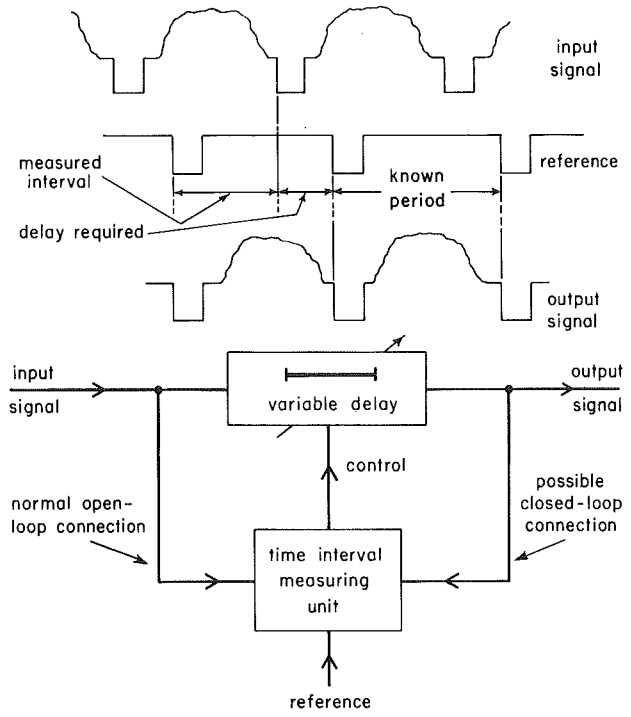

Fig. 1 - Basic variable delay timing corrector

3. The new timing corrector — broad design philosophy

The basic requirement was for a delay with a maximum capacity of about 32 μs, automatically controlled at a rate not exceeding line frequency, so as to correct timing errors to an initial target accuracy of ±10 ns for a monochrome signal, or ±1 ns for a composite colour signal. It was not necessary for the delay to vary during the active line period since the maximum accumulated timing error during this period (or so-called 'velocity' error) was negligibly small.* The basic principle of the variable-delay type of timing corrector is depicted in Fig. 1 which shows the two essential components arranged in the form of an open-loop servo system. A high-speed closed-loop system is not practicable because the delay introduced in the signal path would not permit the required speed of response from the system.

Preliminary considerations indicated that it would not be practicable to achieve the required range and accuracy of timing correction in one stage. To cover the large range, it would be necessary to use a switched delay system comprising a combination of fixed ultrasonic fused-quartz delays and cable delays operating at radio frequency. These would be arranged in binary-related durations with intervening switches such that the effective delay could be varied in increments equal to the smallest delay from zero to a maximum equal to the sum of all the delays. In theory a chain of fifteen delays ranging from say, 16 μs duration for the largest delay to about 2 ns for the shortest, would provide the necessary range and accuracy. In practice however, such a system would present insurmountable difficulties.

The first and major difficulty is that the effective delay values would have to be inter-related to an accuracy commensurate with the smallest delay (2 ns), the extremely precise relationship being maintained regardless of variations in temperature and possible long term effects such as 'creep' in cables or changes in delay time through the associated switches. This would be quite impracticable, particular difficulty arising with the larger delays since the equalised group delay characteristics of quartz delays set a limit of about ±10 ns to the accuracy to which they can be adjusted and maintained. A second difficulty arises in the control of the variable delay. To derive a control signal involves the measurement of the time relationship between a stable reference and the input video signal to the variable delay. With the postulated delay system this would require a time interval of up to about the duration of a television line (64 μs) to be measured to an accuracy of ±1 ns (i.e. to an accuracy of about ±1½ parts in 10^5). The only practicable way to do this is to employ a pulse-counting technique. In this a digital counter is arranged to count the number of 'clock' pulses occurring in the given periods (as defined by the timing reference and the video signal) from a stable oscillator precisely related in frequency to the smallest delay quantum (2 ns). A free-running oscillator could be used to provide the clock-pulse frequency; this would need to run at about 500 MHz with the consequent need for very high speed counters,** but would have the advantage that the frequency stability required (say 3 parts in 10^6) could fairly easily be achieved using crystal control. Alternatively, by using a pulsed oscillator to generate a train of clock pulses having a prescribed phase relationship with the start of the time interval to be measured, the same resolution would theoretically be achieved with a clock pulse frequency reduced by a factor of two, i.e. to 250 MHz. In this case, however, the oscillator could not be crystal controlled (since the high effective 'Q' factor would not permit rapid starting) and severe practical difficulties would arise in meeting the frequency stability requirement. Moreover it is very unlikely that the starting phase of the oscillator could be made sufficiently constant, say to within ±0·2 ns.

For the reasons stated it was decided that the timing corrector should be split into two main stages, in effect, a coarse corrector followed by a fine corrector.

The first stage (designated Timing Corrector 1) would be of the type already described, a chain of binary-related delays, but limited to nine delays, the values such that the total delay was about 33 μs. The system would operate directly on the radio-frequency, frequency-modulated signal emerging from the Main Store. The required clock-pulse frequency would be about 8 MHz, thus no serious difficulties were envisaged with the controlling digital logic. The target accuracy of this first stage was ±33 ns (the duration of the shortest delay being 65 ns) and it was considered that the development of an 8 MHz pulsed oscillator[8] of adequate performance was practicable.

* The maximum accumulated error is about 0·1° of subcarrier phase. This occurs when converting signals from, say, a German PAL source which conforms to System G and is at one extreme of its frequency tolerance range (say −5 Hz at subcarrier frequency) to an output standard which is at the opposite end of the NTSC frequency-tolerance limit (say +10 Hz at subcarrier frequency).

** When the design of the timing corrector was under consideration counters with this speed of operation were not practicable.

It was decided to divide the second (fine) stage of timing correction into two further stages operating successively on the video signal obtained by demodulating the r.f. signal from Timing Corrector 1 (TC1). The first of these (designated Timing Corrector 2) would reduce the incoming timing errors from TC1 to a spread sufficiently small to be acceptable for monochrome pictures. A target accuracy of ±5 ns, corresponding to one-tenth of the duration of a picture element, was therefore chosen. A range of delay variation of 300 ns was thought to be adequate to accommodate both the input timing errors (nominally ±33 ns) and the changes of mean timing arising from inevitable system drifts.

The final stage (Timing Corrector 3) was necessary to reduce the errors still further to a level at which the hue errors (resulting from the chrominance signal phase perturbations) on the NTSC coded colour signal would be acceptably low. The target accuracy chosen was ±1 ns corresponding to a phase error of ±1·6° at the 4·5 MHz colour subcarrier frequency, based on the results of subjective tests made to determine the effect of such perturbations.[9] A delay range of 60 ns was considered sufficient to accept the ±5 ns timing errors expected from TC2 when the equipment was operating as a field-store standards converter. It was realised at the outset that this would be too small to cope with certain problems which would occur when synchronising PAL-coded colour signals (to be discussed in detail later) but it was considered that these would best be overcome by interposing an auxiliary stage (designated Timing Corrector 2A) between Timing Correctors 2 and 3.

It is to be noted that the proposed ratio of delay range to target output timing accuracy (viz. 30 : 1) was the same for both Timing Correctors 2 and 3. The common ratio was deliberately chosen so that the delay-controlling electronics for the type of variable delay envisaged could be largely identical in both correctors, thus minimising the required development effort.

Two possible forms of variable video delay were considered for Timing Correctors 2 and 3. These were an infinitely-variable system consisting of a lumped-constant line, the delay being controlled by varactor diodes, or alternatively, a lumped-constant line of fixed delay with 31 taps at equal intervals, the delay variation being obtained by switching from tap to tap.

The first method has the advantages that unlike the tapped delay, the accuracy of timing correction is not fundamentally limited and the associated electronics controlling the delay might be relatively simple. Also it was clear that fairly complex (albeit repetitive) logic would be necessary to control the 31 taps involved in the tapped-line proposal.

It was decided however, that the infinitely-variable delay presented considerably more difficult development problems than the tapped delay. The problems of particular concern were:

(a) the delay itself, which would be fairly complex with the need, perhaps, to grade and select the varactor diodes.

(b) the non-linear relationship between the delay time and the varactor diode control voltage, (a fourth-power law is involved with consequent difficulty in achieving precise tracking between the measured time error and the correcting delay time.

(c) the need to provide a tracking frequency-response equaliser to compensate for the inevitable change in response as the delay was varied.

(All these problems have, of course, been met by the Ampex* organisation in the production of the well-known 'AMTEC' and 'COLORTEC' timing corrector units in video tape recorders. Indeed the use of these units in the C06/508 equipment was contemplated but ruled out on the grounds of expense, their unnecessarily large timing range, and the fact that considerable detail modifications would have been necessary to adapt them to the different requirements. Moreover, the stated performance** of the Ampex units were poorer than that which it was hoped to achieve.)

It was decided to develop two tapped-delay type correctors, basically similar in form with virtually identical tap-control logic; one would have a range of 300 ns variable in 10 ns steps, the other a range of 60 ns variable in 2 ns steps.

4. The problems when synchronising PAL-coded colour signals

The first two stages of the timing corrector (TC1 and TC2) operate by comparing the relative timing of station reference syncs and a special luminance timing edge (related to the synchronising pulses) on the input video signal. For colour timing correction, however, the third stage (TC3) must compare the phase of the colour burst on the input video signal with that of a reference subcarrier. In the conversion mode of the equipment, there is a fixed relationship between the luminance timing edge and the colour-burst phase, as determined by the intermediate colour coding system,[5] so that only a small range of timing correction is required in TC3 to accommodate the residual errors from TC2. When synchronising PAL colour signals however, which pass directly through the equipment, two problems arise which effectively require the range of TC3 to be much greater.

First, in the PAL system there is no specified relationship between the phase of the colour burst and the timing reference provided by the line-synchronising pulses. Thus, in order to cope with PAL signals from *any* source the colour timing corrector must have a range of at least a full cycle of colour subcarrier (226 ns).

Furthermore, when the Main Store of the synchroniser has to omit or duplicate one television field, this process can involve a 180° change in subcarrier phase of the signal emerging from TC2 which the colour timing corrector must also be able to accept.

* Ampex Corporation, Redwood City, California.

** The specified performance is that the residual timing errors are ±30 ns or less from AMTEC and ±2·5 ns from COLORTEC.

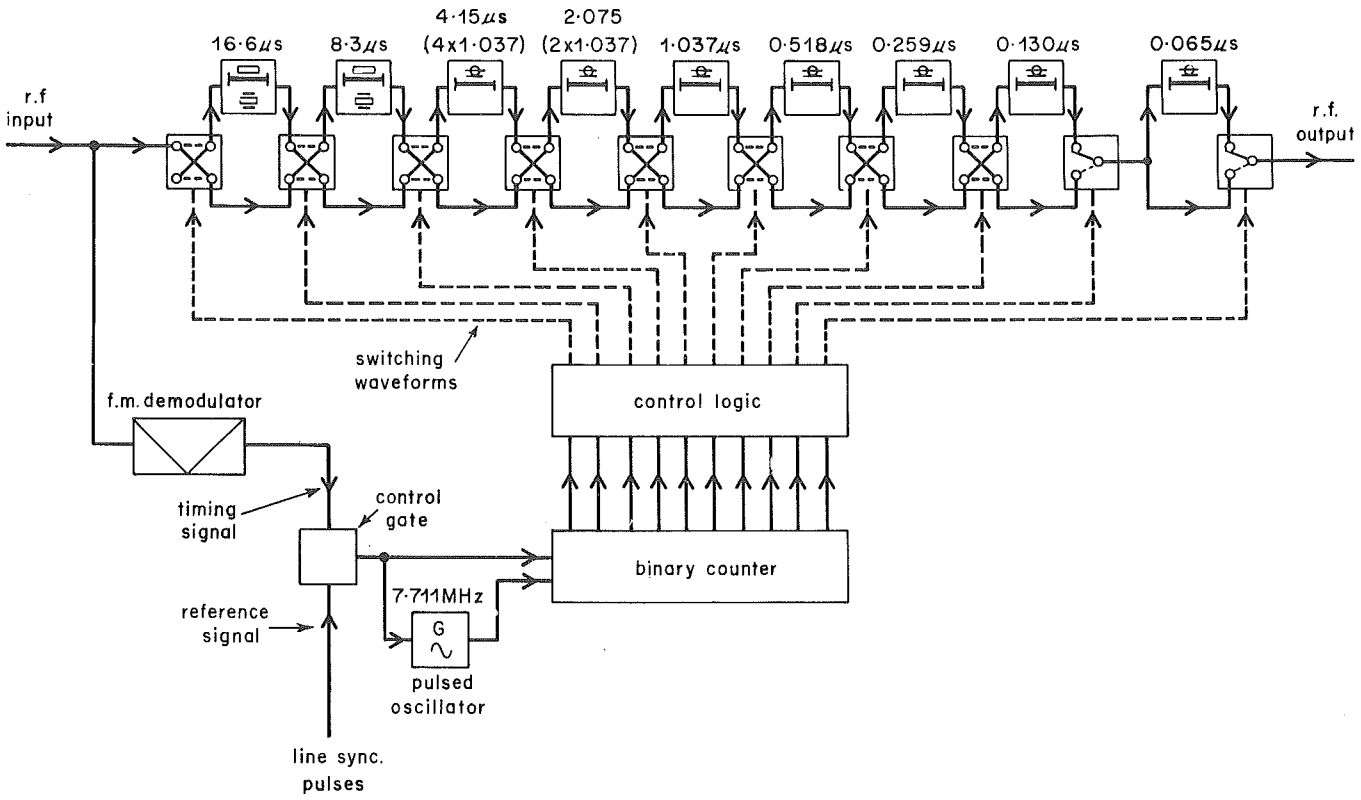

Fig. 2 - Block diagram of timing corrector No. 1

The form of TC3 was suitable for only a relatively small range of timing correction and it was decided that the large range required for the synchroniser mode would best be obtained by interposing an auxiliary timing corrector (TC 2A) between Timing Correctors 2 and 3. This operates at a rate not exceeding field frequency and consists of a chain of binary-related video delays with a setting accuracy of about ±3·5 ns.

It is useful at this point to summarise as in Table 1 the delay ranges and increments of the timing correctors as envisaged when development was started.

TABLE 1

Stage	Range	Increment
1	33 μsecs.	65 ns
2	300 nsecs.	10 ns
2A	330 nsecs.	7 ns
3	60 nsecs.	2 ns

5. Description of each stage

All four stages of timing correction operate in the same basic way; the timing error is measured, and an appropriate delay is inserted in the signal path. Each stage functions in an open-loop mode, although stage 2A has a degree of closed-loop control and there is partial closed-loop operation of stages 2 and 3 together. These modes are described in greater detail below.

5.1. Timing Corrector 1 (TC1)

The signal path consists of a system of delays operating at radio-frequency with a binary relationship from 65 ns to 16·6 μs. The total capacity is thus 33·2 μs. Two of these delay units are of fused-quartz type, namely 16·6 and 8·3 μs, all the remaining units are of cable. The interconnecting systems allow any combination of delays to be selected leaving all other delays connected in a second route. The particular values of delay were chosen for compatibility with delays used in the Main Store. Fig. 2 is a block diagram showing the main features of TC1.

The advantage gained by operating at radio frequency rather than baseband is that it would be difficult to realise and equalise, at baseband, delays of the size required. Also, existing technology as used in the Main Store of the equipment could be used.

The switches are controlled by a logic system which converts the timing error to be corrected into waveforms suitable for switch operation. The error measurement is made by counting the number of 'clock' pulses of a 7·711 MHz pulsed (phase-locked) oscillator in the interval between a timing reference (local sync pulse) and a timing edge (associated with line syncs) derived from the frequency-modulated radio-frequency signal.

A pulsed oscillator was used rather than a free-running crystal oscillator since it could be guaranteed to have a coherent phase relationship with the error-measuring process. The equality of the oscillator period and the delay increment (65 ns) directly affects the corrector output timing accuracy; a pulsed oscillator of sufficient stability was difficult to develop but has proved adequate in service.[10]

The arrangement of switches and delays is such that there are no constraints on the delay required for successive television lines (provided that they are within the 33 μs range), and each switch is operated at a time determined by the position of that switch and the delay state from which TC1 is changing. The use of a binary cascade of switched delays makes it possible to change the timing of the signal progressively from that required for one line to that required for the next without interrupting the flow. It is interesting to compare this arrangement of delays with that used in the Ampex AVR1 timing corrector, which is restricted in the acceptable line-to-line timing errors to a maximum of 1 μs.[11]

For several reasons the design performance of ±33 ns output timing accuracy was not achieved. Degradation of this performance is due to:

1) noise in the timing measurement
2) clock-pulse frequency errors
3) clock-pulse starting phase errors
4) delay errors

Incorrect delay values were found to constitute the main source of timing error; the overall timing accuracy is ±50 ns.

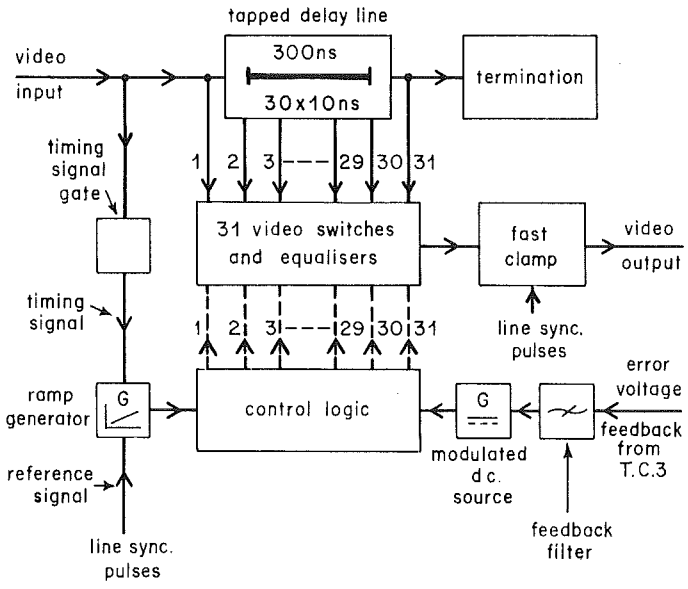

Fig. 3 - Block diagram of timing corrector No. 2.

5.2. Timing Corrector 2 (TC2)

Fig. 3 is a block diagram showing the main features of TC2.

The signal path consists of a 300 ns lumped constant, video delay line, tapped at 10 ns intervals giving 31 taps. At each tapping point there is a simple video switch and equaliser which feeds into a collecting point to form the delayed signal output. The delay inserted, therefore, is determined by the tap selected.

Tap selection is made by the control logic which compares the input signal timing edge (as in TC1) with a local reference signal derived from line syncs. This is accomplished by allowing a linear voltage ramp to run during the interval between these two signals and applying the stopped ramp voltage to an analogue-to-digital converter. The digital measurement thus obtained is stored and code-converted to a form suitable for operating a particular video switch. The analogue-to-digital converter has 30 comparators, which compare the ramp signal with 30 d.c. voltages derived from a bias supply. This d.c. bias is modified by a feed-back signal from TC3, this will be explained in more detail below.

The video signal undergoes certain distortions as a result of the delaying process, the most important are:

(1) a line-rate (box-car) component which is added by the video switches due to imperfect transistor matching.

(2) dispersion at high frequencies which occurs due to the varying frequency response of the delay line.

The first distortion is removed by a fast clamp operating on the signal after timing correction. This re-establishes the blanking level of each television line by clamping during the back porch.

The second distortion arises from the simple equalisation introduced at each tap. Each video switch feeds its output into the collecting point via a shunt resistor and capacitor circuit which provides a degree of equalisation but which inevitably introduces some phase shift at high frequencies. A reasonable compromise produces a fairly consistent frequency response (range ±½ dB at 5 MHz) with an effective shortening of the delay line of only 25 ns at 4·5 MHz.

For the following reasons the design performance of ±5 ns output timing accuracy was not achieved:—

(1) the effect of noise on the signal timing edge

(2) small mismatches between the slope of the voltage ramp and the delay line increments

(3) errors in the ramp start and stop timings.

In practice, an output timing accuracy of ±10 ns is achieved, the degradation being almost entirely due to the effect of noise.

5.3. Timing corrector 3 (TC3)

Fig. 4 is a block diagram of TC3 showing its main features. The signal path consists of a 60 ns lumped-constant video delay line, tapped at 2 ns intervals giving 31 tapping points. At each tap there is a simple video switch (as in TC2) feeding directly into a collecting point. Equalisation is unnecessary since the delay line has little loss at high frequency, the cut-off frequency being about 75 MHz.

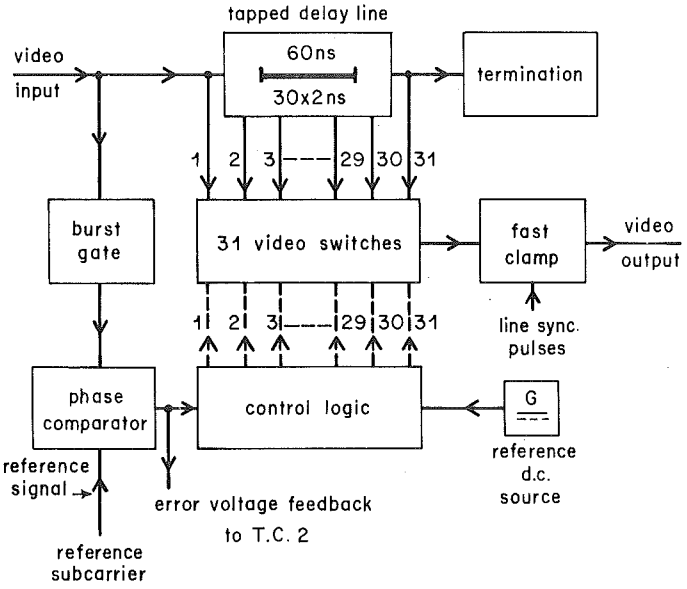

Fig. 4 - Block diagram of timing corrector No. 3

Tap selection is made by the control logic which compares the phase of the colour burst on the signal to be corrected with that of a reference subcarrier. A sawtooth waveform is generated in synchronism with the reference subcarrier, and is sampled at the zero crossings of the colour bursts of the incoming video signal. The resulting voltage, linearly proportional to the phase difference, is presented to an analogue-to-digital converter, the digital measurement being stored and code converted as in TC2, to energise a selected video switch.

Although the timing error measurement is based on phase comparison, whilst the correction is by means of delay, the difference in the subcarrier frequencies (4·5 MHz for conversion, 4·433 MHz for synchronisation) does not produce significant errors.

As in TC2, a line-rate component is added to the delayed signal by the video switches; this is removed by a fast clamp, operating in a special period of blanking between the colour burst and the start of the active line.

A form of negative feedback of error signal is used between TC3 and TC2. This is designed specifically to remove the large, low-frequency chrominance phase errors associated with group delay distortions in the Main Store and not fully removed by TC2 which operates on a luminance timing edge. In the convert mode, the Main Store delays are switched systematically, producing a rapidly changing group delay characteristic, which increases the timing errors which TC3 has to handle. Accordingly, the phase error signal (which is of box-car form) is band-pass filtered to pass energy in the range 30 to 300 Hz approximately, and is applied to the reference bias used in the timing measurement process in TC2. This modifies the ramp measurement and changes the tap selection in such a way as to reduce the range of burst phase errors emerging from TC2. The gain and time constants are chosen to prevent oscillation of the combined system, which includes the intervening Timing Corrector 2A (TC 2A) as a varying propagation delay. Using this technique, the range of phase errors in the signal emerging from TC2 is reduced by approximately 40 percent.

The design performance of ±1 ns output timing accuracy was not achieved, largely due to noise and interfering signals affecting the phase measurement. In practice, an output timing accuracy of ±2·5 to ±3 ns was achieved, although measurement of these figures is made difficult by noise on the video signal. The resulting impairment is not excessive and is noticeable only on the most stringent programme material.

5.4. Timing corrector 2A (TC2A)

The primary function of TC2A is to control the input signal timing to TC3, in such a way that TC3, which has only a 60 ns correction range, is always range-centred. In the synchronising mode (for the reasons given in Section 4) the signal from TC2 may have any mean phase relationship with reference subcarrier, and so TC2A requires a delay capacity of at least 226 ns (360° phase). Also the omission or duplication of one field in the Main Store causes a 180° phase change in colour subcarrier which must be removed before signals can be fed to TC3. A secondary function of TC2A is to correct for system drifts in subcarrier phase.

As shown in Fig 5 the signal path consists of binary related delays from 113 ns (180°) to 6·7 ns (11¼°). A second 113 ns delay is included to extend the delay capacity to 330 ns (540°).

The timing corrector operates by a series of successive approximations. Each delay is associated with a phase detector which determines whether the colour burst phase leads or lags that of the reference subcarrier. Measurements are integrated over several television lines to reduce the effects of noise. Depending on the measurements, the delay is inserted or removed by means of a video switch. Delay changes are permitted to occur only at the end of the field-blanking interval and the method of operation is such that up to five fields may be required initially to achieve full phase correction of the video signal to within $\pm 5^{5}/_{8}°$. Thereafter, input errors at a rate of up to 11¼° per field are corrected.

The rate of operation of TC2A is limited to field frequency to ensure proper operation of the closed-loop feedback system embracing TC2, TC2A and TC3 (described in Section 5.3).

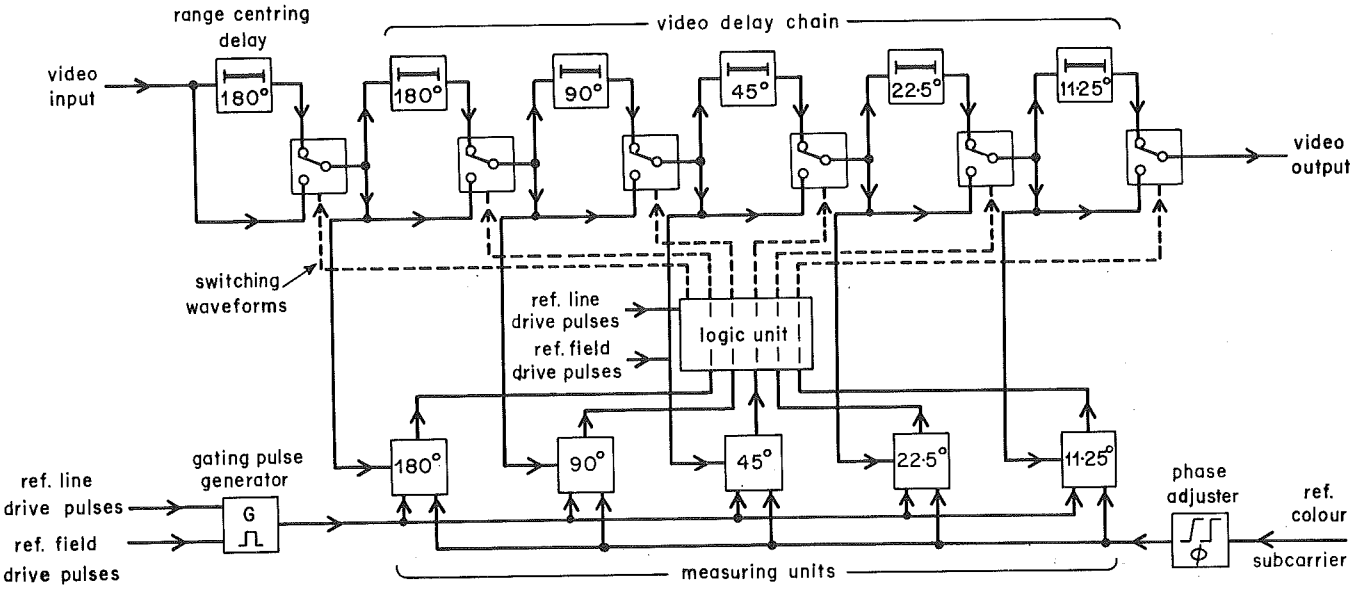

Fig. 5 - Block diagram of timing corrector No. 2A

When a field is omitted or duplicated (in the synchronise mode of operation) TC2A can be presented with a 180° change in the burst phase. Correction of this is accomplished within one field by special logic circuits which detect the 180° phase change and allow only the 180° delay to be switched in or out as required.

The larger delays are automatically modified by means of small switched delays, to compensate for the different subcarrier frequencies i.e. 4·5 MHz when converting and 4·43 MHz when synchronising, thus preserving an accurate relationship between the phase error detection and compensation.

Since, in TC2A, the control signals are derived from measurements of phase and the subsequent correction is by means of delay a situation can arise where a delay equivalent to 349° and a delay equivalent to 0° are alternating due to measurement errors or noise. This would produce unacceptable timing errors of about 220 ns of picture information. The inclusion of the second 180° unit obviates this condition, allowing the delay to increase towards 540°. A range-centering circuit ensures that at all times, this hunting state is avoided.

In practice, the design performance was achieved, TC2A reduces the signal colour burst phase errors until they are within $\pm 5^{5}/_{8}°$ (±3·4 ns) of the nominal reference phase. If the mean phase of the incoming signal changes by more than 11¼° per field the change cannot be completely removed, but will always be reduced. In this way TC2A can take out a subcarrier frequency error of up to ±1·5 Hz by continuously increasing or reducing its delay. This situation arises when an incoming PAL signal is to be synchronised but its subcarrier is not correctly related in frequency to its line rate. Under these conditions, TC2A sets its delay so that the subcarrier phase is correct at the beginning of each field.

Conclusions

The target accuracy of timing correction was not achieved in Timing Correctors No. 1, 2 and 3, largely because of noise and signal distortions originating in the Main Store of the Field-Store Standards Converter/Synchroniser. Primarily, noise affects the timing processes used in TC1 and TC2, while signal distortions affect the chrominance phase measurement in TC3. The main signal distortions are dispersion which effectively gives different timings for the luminance and chrominance components of the video signal, and breakthrough from input to output of the Main Store delay units, which adds random phase errors to the signal colour burst.

The achieved performance of the complete Timing Corrector, while falling short of the target in some respects has been found satisfactory in practice and compares favourably with that of the timing correction system as used by the Ampex AVR1.[10]

With hindsight, several alternative approaches to timing correction would be possible. The first involves a revision of the techniques used; a second would use digital techniques to accomplish full timing correction in one stage.

The most attractive alternative would be to extend the range of TC1 from ±16 μs to ±32 μs (one television line). This could increase the input frequency tolerance of the Field-Store Standards Converter/Synchroniser, in the synchronise mode, from $\pm 5{\cdot}5 \times 10^{-4}$ to $\pm 1 \times 10^{-2}$ or possibly even greater. This is possible since TC1 could omit or duplicate lines as required, the only limitation then being the length of the active line, which could not be corrected.

The use of a binary-related chain of delays, either at r.f. or at video frequencies is a possible alternative to the

distributed delay used in TC2. This offers no operational advantages but may result in a lower level of signal distortion.

A binary chain of delays could again be used in TC3 having a range of two subcarrier periods, thus rendering the intermediate stage TC2A redundant. Only nine delay sections would be required with switches, the resulting equipment would certainly be no larger than the existing TC2A and TC3 together.

The alternative approach of an entirely digital timing corrector is the more attractive, since it would not degrade the signal in any way. Such a timing corrector would merely store each television line emerging from the Main Store, and deliver that line correctly timed and of the correct length. Two television line stores would be required, since reading and writing of different information would be performed simultaneously. Any future timing correction applications will almost certainly use this technique. The variable delays in a digital timing corrector might consist of shift registers which introduce binary-related delays; much of the design philosophy discussed in this report will therefore continue to be relevant.

7. References

1. A field-store converter using ultrasonic delays as the storage medium. BBC Research Department Report No. T-136, Serial No. 1964/65.

2. Field-store standards conversion: conversion between television signals with different field frequencies using ultrasonic delay lines. BBC Research Department Report No. T-164, Serial No. 1966/12.

3. Field-store standards conversion: description of the C06/508 converter. BBC Research Department Report No. 1970/37.

4. An outline of synchronous standards conversion using a delay-line interpolator. BBC Research Department Report No. T-096, Serial No. 1962/31.

5. BBC Research Department Report in course of preparation.

6. BBC Research Department Report in course of preparation.

6. Field-store standards conversion : the field-store synchroniser. BBC Research Department Report No. 1971/38.

7. BBC Research Department Report in course of preparation.

8. BBC Research Department Report in course of preparation.

9. The impairment caused by phase-perturbation of the colour sub-carrier in a colour television system of the NTSC type. BBC Research Department Report No. EL-16, Serial No. 1968/11.

10. BBC Research Department Report in course of preparation.

11. COLEMAN, C.H. 1970. A new technique for time-base stabilization of video recorders. *I.E.E.E. Trans. Broadc.*, 1971, **BC-17**, 1, pp. 29 – 36.

SMW/JUC

Printed by BBC Research Department, Kingswood Warren, Tadworth, Surrey